Energy-Band Engineering for Tunable Memory Characteristics through Controlled Doping of Reduced Graphene Oxide

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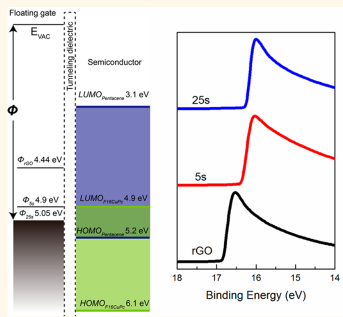
ABSTRACT Tunable memory characteristics are used in multioperational mode circuits where memory cells with various functionalities are needed in one combined device. It is always a challenge to obtain control over threshold voltage for multimode operation. On this regard, we use a strategy of shifting the work function of reduced graphene oxide (rGO) in a controlled manner through doping gold chloride ($AuCl_3$) and obtained a gradient increase of rGO work function. By inserting doped rGO as floating gate, a controlled threshold voltage (V_{th}) shift has been achieved in both p- and n-type low voltage flexible memory devices with large memory window (up to 4 times for p-type and 8 times for n-type memory devices) in comparison with pristine rGO floating gate memory devices. By proper energy band engineering, we demonstrated a flexible floating gate memory device with larger memory window and controlled threshold voltage shifts.



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In logic circuits, various operational modes are expected to be assembled in a circuit so that multifunctionality is possible within one integrated circuit (IC). Lower threshold voltage (V_{th}) for transistors can be used in noncritical paths to reduce the static power (minimizing overall leakage power), while higher V_{th} transistors can be used in performance-critical paths to meet performance requirements. In addition, tunable memory characteristics (various V_{th} of programmed and erased states) can be utilized in multilevel storage circuits (such as NOR and NAND gate flash) where memory cells with different bits are needed in one combined device. Thus, an adjustable V_{th} is highly advantageous not only for control over operation mode in logic circuit but also for various data storage applications. In general, V_{th} of the flash memory device can be tuned *via* a change in channel conductance by stored charges in floating gate.[1,2] To meet stringent requirements of low power consumption, high integration density and fast access speed, nanofloating gates are considered as the most promising candidates to replace the planar floating gates for next generation flash memory devices.[3−9] Tuning the memory characteristics by direct energy band engineering of the charge trapping layer has its own niche due to gradient control over the Fermi level of the floating gate. However, the nanofloating gate flash memory based on metal nanoparticles such as gold nanoparticles (Au NPs) could not achieve tunable memory characteristics by energy band engineering due to its fixed Fermi level.[10−13] On this regard, we chose graphene which is a two-dimensional (2D) material with layered structure and its Fermi level can be manipulated.[14] Various methods were proposed to tune the work function of graphene including doping of foreign atoms (boron for p-doping and nitrogen for n-doping),[15,16] dipole moment arising from self-assembled monolayer (SAM) and chemical doping.[17−19] Adsorption-induced chemical doping was considered as an effective way to shift the Fermi level of graphene by charge transfer between the

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graphene sheets and adsorbed species without introducing substitutional impurities and additional damage to carbon network. On this aspect, gold chloride ($AuCl_3$) can be chemically adsorbed to add high work function Au metal on graphene to shift the Fermi level of graphene downward since the positive Au^{3+} can be spontaneously reduced to zero charge (Au^0) by capturing electrons from graphene due to their negative Gibbs free energy.[17−20] There are relatively few reports describing the doping of reduced graphene oxide (rGO).[21] The incompatibility of chemical vapor deposition (CVD) method with high yield and low cost mass production makes rGO become more and more attractive even though unavoidable lattice defects induce slight degradation of its electrical properties.[21] Tremendous progress has been achieved on the fabrication of various kinds of memory devices based on graphene and its derivatives.[23−31] However, tunable memory characteristics by tuning the Fermi level of rGO as floating gate has not been reported elsewhere which is important for various applications such as in multilevel data storage circuits. In addition, we have achieved large memory window (up to 4 times for p-type and 8 times for n-type memory devices) by tuning the Fermi level of rGO through chemical doping which is much wider than our previous reports on Au NPs single floating gate memory device and rGO sheets-Au NPs hybrid double floating gate memory device.[5]

Here, we demonstrate a low voltage flash memory based on $AuCl_3$ doped self-assembled rGO floating gate on flexible polyethylene terephthalate (PET) substrate. The pentacene and copper hexadecafluorophthalocyanine ($F_{16}CuPc$) were employed as p-type or n-type semiconductors, respectively. By embedding rGO monolayer with various doping concentration of $AuCl_3$ (as a function of doping time of 0 s, 5 s, 25 and 45 s) between aluminum oxide (Al_2O_3) (blocking dielectric layer) and poly(methyl methacrylate) (PMMA) (tunneling dielectric layer), the memory characteristics have been systematically controlled in both p-channel and n-channel memory transistors. Compared with a standard flash memory fabricated on pristine rGO monolayer, the memory window is found to be significantly improved with an increasing doping concentration of $AuCl_3$. As the doping time increases to 25 s, a largest memory window is obtained in both p-channel and n-channel flash memory (up to 4 times for p-type and 8 times for n-type memory devices) while increasing the doping time up to 45 s displays rough surface morphology with inferior device performance. X-ray photoemission spectroscopy (XPS) was used to characterize the doping process. Atomic Force microscopy (AFM) was used to examine the surface of the $AuCl_3$-doped rGO layer. The change of work function of rGO after metal chloride doping was confirmed by ultraviolet photoemission spectroscopy (UPS). Charge carrier injection barrier has been lowered through better energy level alignment between the Fermi level of doped rGO layer and HOMO level of pentacene/$F_{16}CuPc$. The downward shift of Fermi level of rGO and increased size and density of reduced Au NPs have a synergistic effect over the significant enhancement of the memory window. Meanwhile, various V_{th} have been achieved in both p- and n-type memory devices fabricated on rGO with controlled doping concentration of $AuCl_3$. In addition to large memory window and controlled V_{th} shifts, the chemically doped rGO floating gate memories exhibited fast program/erase speed (100 ms), long retention time (10^5 s), good endurance properties (>800 cycles) and mechanical stability (>500 bending cycles). Furthermore, our fabrication methods including synthesis of rGO sheets, the self-assembly of rGO monolayer and $AuCl_3$ doping are all solution-processed at low temperature, and have been extended on flexible substrates for the construction of innovative graphene electronics.

RESULTS AND DISCUSSION

Graphite oxide was synthesized from natural graphite (SP-1) by the Hummers method.[32] After converting the graphite oxide to GO by ultrasonication, the well-dispersed negatively charged rGO sheets were achieved by hydrazine reduction of GO with the presence of ammonia in water.[33] The AFM image of single rGO sheet and Raman spectrum evidencing significant structural variation from GO to rGO after the chemical reduction are depicted in the Supporting Information. The rGO sheets display lateral dimension of around 1−2 μm and an effective thickness of ~1 nm.

The AFM images indicating the effect of $AuCl_3$ doping time on the surface morphology of doped rGO and pristine rGO film are shown in Figure 1a−c respectively. The increased size of Au NPs and respective morphological changes could be observed due to longer doping time. Higher reduction potential of $AuCl_4^-$ ion than the rGO induces the formation of Au NPs on the rGO film.[18,34] The rGO doped by $AuCl_3$ for 25 s displayed larger and broader size distribution of Au NPs in comparison with 5 s doping time. However, the rGO doped by $AuCl_3$ for 45 s displays rough surface morphology (Figure S2) which is not suitable for device fabrication, and the memory devices based on rGO doped by $AuCl_3$ for 45 s neither have field-effect transistor (FET) properties nor memory performances. Figure 1d,e shows the XPS data of rGO doped with $AuCl_3$ for 5 and 25 s. The spectral line shape was simulated by a suitable combination of Gaussian and Lorentzian functions to separate the chemical bonding states.[35] For all fitting multiplets, the full width at half-maximum (fwhm) values was fixed accordingly. The peaks of doped rGO film are composed of metals (Au) and metal ions (Au^{3+}), while the corresponding peaks cannot be found in the pristine rGO film (Figure S3 in

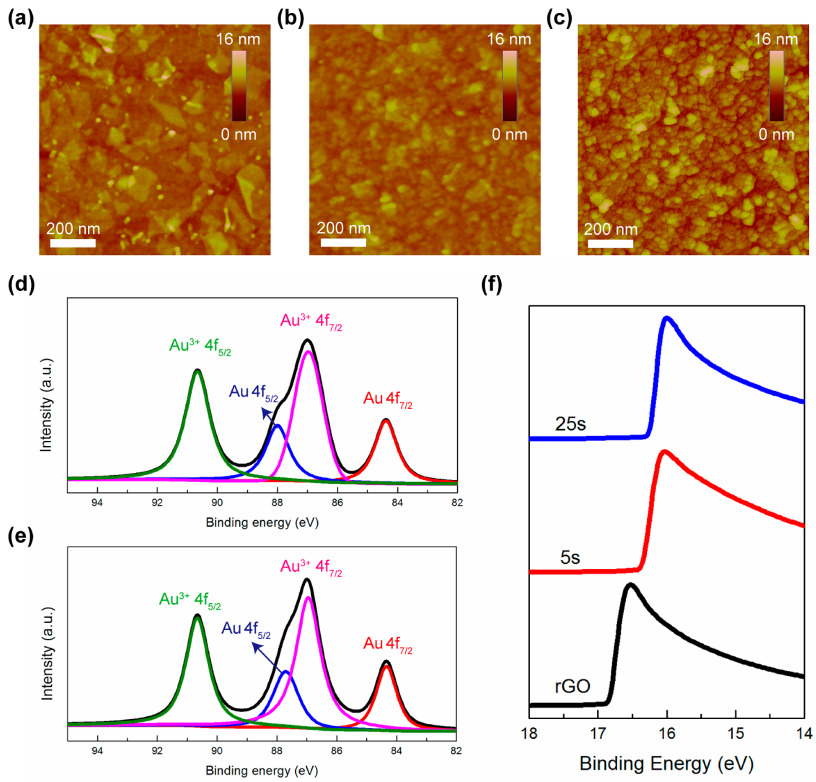

Figure 1. Tapping-mode AFM image of (a) pristine rGO monolayer, (b) rGO doped with $AuCl_3$ for 5 s, and (c) rGO doped with $AuCl_3$ for 25 s. The XPS data (metal peak) of (d) rGO doped with $AuCl_3$ for 5 s and (e) rGO doped with $AuCl_3$ for 25 s. (f) The work function variance between doped and undoped samples were measured by UPS.

Supporting Information) indicating the successful doping process. For XPS measurements, the samples were prepared on precleaned heavily doped n-type silicon substrates to avoid Au doping effect from the substrate. Simply comparing the peak intensity ratio of Au^{3+} to Au cannot confirm the p-doping by electron transfer from rGO sheet to metal ions so that UPS measurements were carried out. Figure 1f shows the UPS spectra around secondary electrons threshold region of pristine rGO film and rGO doped with $AuCl_3$ for 5 and 25 s. A gold plate is used for the calibration. The vacuum level of the samples were determined by linear extrapolating the secondary electron cutoffs on the high-binding energy side of the UPS spectra (14−18 eV).[36] The work function is determined by subtracting E_{SE} from $h\nu$, where $h\nu$ and E_{SE} are the incident photon energy (He I discharge lamp, 21.2 eV) and secondary edge position.[37] The work function of rGO sample is determined to be about 4.44 eV, while the work function of rGO doped with $AuCl_3$ for 5 and 25 s is found to be 4.9 and 5.05 eV, respectively, demonstrating an increased work function with longer doping duration. The work function of all doped rGO is found to be greater than pristine rGO film indicating that $AuCl_3$ is a strong p-dopant.

The bottom-gate top-contact flash memory devices were then fabricated on $AuCl_3$ doped rGO charge trapping layer. The fabrication process is described in Figure 2a. A 25 nm silver (Ag) gate electrode and 40 nm aluminum oxide (Al_2O_3) blocking dielectric layer are successively deposited on the PET substrate by thermal evaporation and atomic layer deposition (ALD), respectively. The positive charged self-assembled monolayer (SAM) is formed by immersing the substrate into a solution of 3-aminopropyltriethoxysilane (APTES). The monolayer coverage with maximum rGO density has been achieved by first-adsorbed rGO pieces followed the Langmuir isotherm mode.[38] The negative charged rGO is allowed to self-assemble for several minutes prior to spin-coating at high speed to form a single layer film (seen in Figure 1a). The substrate with rGO sheets monolayer is then immersed into $AuCl_3$ aqueous solution with a concentration of 5 mM for various durations (5 and 25 s). After the construction of $AuCl_3$ doped rGO floating gate, another 25 nm PMMA layer is spin-coated on the floating gate as tunneling dielectric layer. Finally, p-type pentacene/n-type $F_{16}CuPc$ and 30 nm Au are thermal evaporated as active layer and source/drain electrodes, respectively. The optical image of the flexible memory is depicted in Figure 2c.

To realize the enhancement of flexibility of flash memory with Al_2O_3 blocking dielectric layer, suitable selection of tunneling dielectric layer is very important. Furthermore, the overall device performance and reliability are determined by tunneling dielectric layer. Here, we choose PMMA as tunneling dielectric layer due to its various advantages such as high resistivity, thermal/mechanical stability, easy processability,

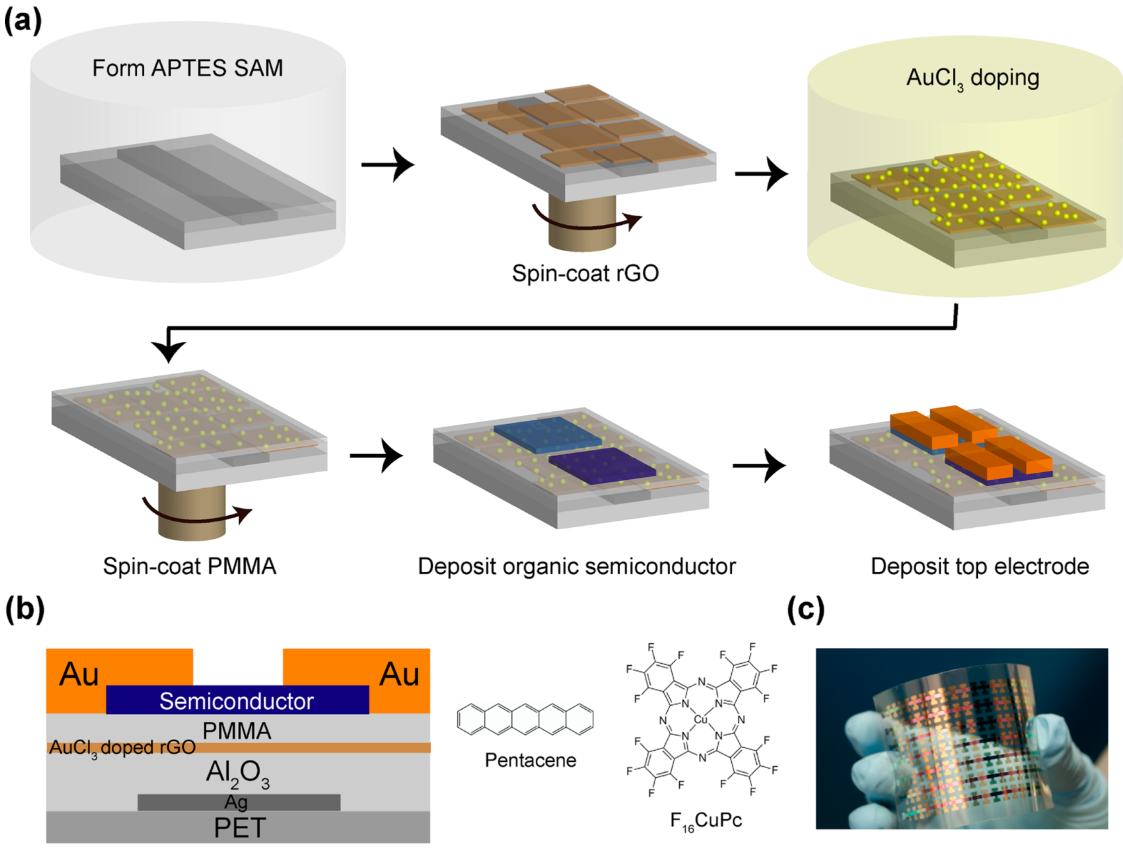

Figure 2. (a) Schematic diagram depicting the basic fabrication process of $AuCl_3$ doped rGO floating gate memory device. (b) Fabricated device structure for memory device with inserting $AuCl_3$ doped rGO floating gate and molecular structure of pentacene and $F_{16}CuPc$. (c) The optical image of the flexible memory.

compatibility with organic molecule growth and low annealing temperature.[39,40] As the active layer of flash memory, both p-type pentacene and n-type $F_{16}CuPc$ were chosen to present the charge trapping effect of $AuCl_3$ doped rGO floating gate separately. Figure 3a,e shows the transfer characteristics of the standard n-channel and p-channel FET devices without charge trapping layer (device structure: PET/Ag/40 nm Al_2O_3/25 nm PMMA/pentacene or $F_{16}CuPc$/Au source-drain). Unless otherwise mentioned, the electrical characterization of all the devices was carried out in ambient conditions. The standard devices exhibited negligible charging/discharging behavior after applying the gate bias pulses of −8 V/+8 V for 1 s, indicating almost no charge trapping in the bulk and interfaces of dielectric layers. It is worth noting that APTES has almost no memory effect within short writing time.[1,11] The p-channel standard transistor exhibited a mobility (μ) of ~0.2 $cm^2\ V^{-1}\ s^{-1}$ and on/off ratio (I_{on}/I_{off}) of ~1×10^4, while the n-channel standard transistor displayed a μ of ~2×10^{-3} $cm^2\ V^{-1}\ s^{-1}$ and I_{on}/I_{off} of ~2×10^2.

The transfer characteristics of the p-channel memory device (device structure: PET/Ag/40 nm Al_2O_3/rGO or doped rGO/25 nm PMMA/pentacene/Au source-drain) and n-channel memory devices (device structure: PET/Ag/40 nm Al_2O_3/rGO or doped rGO/25 nm PMMA/$F_{16}CuPc$/Au source-drain) at initial state, programmed state and erased state are shown in Figure 3. The transfer curves were obtained by the sweeping of gate voltage after the application of programming/erasing bias pulses at −8 V/+8 V for 1 s. Charge trapping occurred in the memory transistors after the insertion of pristine rGO or $AuCl_3$ doped rGO between the PMMA and Al_2O_3 layers. Direct tunneling (at relatively low voltage) and Fowler-Nordheim (F−N) tunneling (at relatively high voltage) are proposed as the favorable ways to program/erase devices rather than the channel hot electron/hole injection since the low drift velocity are induced by low mobility of pentacene and $F_{16}CuPc$ compared with Si-based transistor.[1,41] For the flash memory based on pentacene channel, the transfer curve shifts toward negative voltage direction in comparison with the initial state, which approves that rGO and doped rGO act as trapping element of holes after the application of negative bias at the gate electrode.[1] Controllable V_{th} shifts of programmed and erased states strongly influence the memory window (ΔV_{th}) which is determined by the number of trapped charge carriers in the floating gate and can be defined as the difference between the V_{th} of programmed state and erased state (V_{th} (programmed) and V_{th} (erased)). The memory windows of the p-channel flash memories

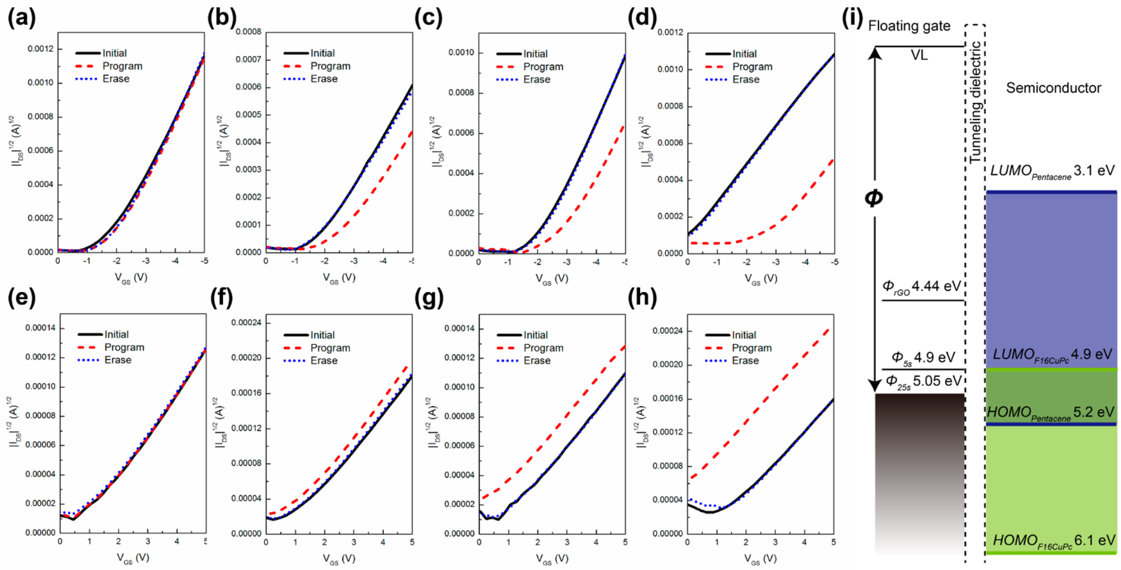

Figure 3. (a) Transfer characteristics of a standard p-channel pentacene FET device. Memory characteristics of flash memories based on (b) pristine rGO film, (c) rGO doped with $AuCl_3$ for 5 s, and (d) rGO doped with $AuCl_3$ for 25 s. (e) Transfer characteristics of a standard n-channel $F_{16}CuPc$ FET device. Memory characteristics of flash memories based on (f) pristine rGO film, (g) rGO doped with $AuCl_3$ for 5 s, and (h) rGO doped with $AuCl_3$ for 25 s. (i) Schematic band diagrams of pentacene, $F_{16}CuPc$, and chemical doped rGO.

with the pristine rGO, doped rGO with $AuCl_3$ for 5 and 25 s as floating gates are 0.7, 1, and 2.7 V, respectively. In the case of rGO based flash memory, the charge carriers are stored in the Fermi level of rGO domains surrounded by the band gap of dielectrics which has similar operation mechanism in comparison with metal NPs floating gate type memory.[3,5] GO can replace rGO layer to work in our device structure to form a charge-trap flash memory in which the charges can be stored in the amorphous GO dielectric where oxygen functionalities like epoxy, carboxyl and hydroxyl groups have high electron affinity.[42] However, the memory characteristics of GO based charge-trap flash memory cannot be manipulated by Fermi level engineering due to its different charge storage mechanism in comparison with the rGO based floating gate flash memory. The narrow memory window of pristine rGO floating gate flash memory may be originated from large charge carrier injection barrier due to the mismatch of the Fermi level of rGO (4.44 eV) and HOMO level of pentacene (5.2 eV). Memory window gradually increased with the increased immersing time and the memory device based on rGO doped $AuCl_3$ for 25 s floating gate exhibited a relatively broad memory window. These distinctive memory characteristics of the doped rGO memory devices originated from the alignment of energy levels for the charge injection from semiconductor to floating gate. The $AuCl_3$ doped rGO shows p-doped characteristics, thus reducing injection barrier between its Fermi level and HOMO of pentacene (Figure 3i). It is believed that lower injection barrier is essential for efficient charge transfer and trapping of charges at $AuCl_3$ doped rGO floating gate memory device which resulted a large memory window. Besides the work function engineering, doping with Au NPs affects the memory characteristics of the flash memory in several other ways. Primarily, doping of Au NPs can introduce more charge trapping sites that contribute to easier programming operation and large memory window. The charging/discharging behavior can be elucidated by the ionization potential (IP)/electron affinity (EA) of the metals being used.[43] The difference between the IP and EA is the charging energy, which can be calculated by the equation: $e^2/2C$. Where the e is the fundamental unit of charge and C is the capacitance of the particle which is proportional to the diameter of Au NPs. The capacitance of Au NP can be estimated from $C = 4\pi\varepsilon_0\varepsilon_r r$, where ε_0 is permittivity of vacuum, ε_r is the dielectric constant surrounding the nanoparticle, and r is the radius of nanoparticle.[2,44] With longer doping duration, larger and broader size distribution of Au particles is observed in rGO film doped with $AuCl_3$ for 25 s in which the charging energy is smaller than that of rGO film doped with $AuCl_3$ for 5 s since both EA and IP approach bulk work function as the radius of NPs increases.[2] Second, with limited $AuCl_3$ doping time, the Au NPs layer is found to be thin; hence, an interface dipole is formed between the rGO and Au NPs, which enhances the charge-injection process.[18] Finally, the number of trapped holes effectively assists the p-doping process of rGO, which leads to the continuous downward shift of rGO Fermi level.[45] All together, we assume that tunable memory characteristics of memory devices based on doped rGO are originated from coactivation of enhanced work function of rGO, increased size and density of Au NPs, interfacial dipole formation between Au NPs and rGO film and finally trapped positive charge carriers assisted p-doping of rGO films. In Figure S4, high voltage memory device based on rGO doped with $AuCl_3$ for 25 s was also fabricated; the memory window is around 40 V (programming/erasing operation of −80 V/+80 V), which is much higher than those reported memory device based on solution-processed GO/rGO.[42,46]

For n-channel flash memory ($F_{16}CuPc$ as semiconductor layer), interestingly, the transfer curve shifts toward negative voltage direction compared with the initial state implicating that rGO and doped rGO act as trapping element of holes after the application of negative bias on the gate electrode. The memory windows of n-channel flash memory based on rGO, and doped rGO with $AuCl_3$ for 5 and 25 s as floating gates are 0.3, 1.1, and 2.4 V, respectively. The reason for much narrower memory window of n-channel flash memory based on pristine rGO is due to deeper HOMO level of $F_{16}CuPc$ (5.9 eV) in comparison with p-type pentacene eventually leads to low charge carrier injection efficiency (Figure 3i). The insertion of $AuCl_3$ doped rGO as charge trapping layer shows memory characteristics with enhanced memory window for both p-channel and n-channel flash memory. In addition, through doping a control over V_{th} shift has been obtained. The tunable V_{th} values of p- and n-channel flash memory based on rGO with various doping concentration of $AuCl_3$ are summarized in Table 1. The program/erase speed of p-channel and n-channel memory devices based on pristine and doped rGO with 25 s immersing duration are shown in Figure S5 in the Supporting Information. The V_{th} shift is enhanced with increasing programming/erasing operation time. More than 100 ms bias pulse is needed to obtain a large memory window. With an additional Au NPs layer on rGO, the memory device based on chemical doped rGO did not exhibit degradation over program/erase speed compared with pristine rGO memory device, since higher density of Au NPs could produce a lower gate-coupling ratio, which refers to the ratio of voltage drop

TABLE 1. Threshold Voltages of Programmed State and Erased States and Memory Windows with Respect to the Various Doping Concentration of $AuCl_3$ in rGO

	pentacene			$F_{16}CuPc$		
	V_{th} (P)	V_{th} (E)	memory window	V_{th} (P)	V_{th} (E)	Memory window
rGO	−2.3 V	−1.6 V	0.7 V	0.4 V	0.7 V	0.3 V
5 s	−2.7 V	−1.7 V	1 V	−0.3 V	0.8 V	1.1 V
25 s	−2.5 V	0.2 V	2.7 V	−1.4 V	1 V	2.4 V

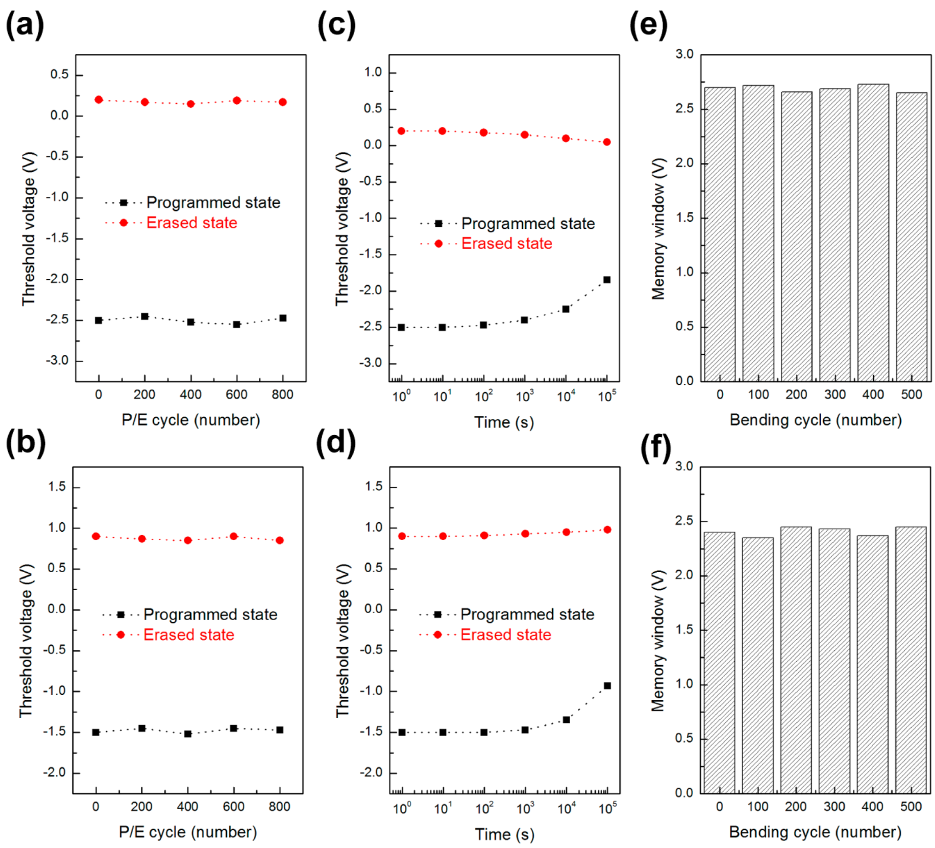

Figure 4. Endurance characteristics of (a) p-channel and (b) n-channel memory device based on rGO doped with $AuCl_3$ for 25 s. Data-retention capability as function of the retention time of (c) p-channel and (d) n-channel memory device based on rGO doped with $AuCl_3$ for 25 s. Mechanical-stability test of flexbile (e) p-channel and (f) n-channel memory device based on rGO doped with $AuCl_3$ for 25 s.

across the tunneling oxide and total voltage across the channel and gate.

Figure 4a,b shows the results of memory cycling endurance test for the p-channel and n-channel flash memory fabricated on doped rGO floating gate with 25 s immersing duration by sequential application of gate biases of −8 and 8 V at V_{DS} of −5 V (p-channel) and +5 V (n-channel), for a series of processes such as writing, reading, erasing, and reading, respectively. These results show reversible and stable memory-cycle behavior for more than ∼800 cycles. Figure 4c,d shows retention characteristics for both p-channel and n-channel flash memory states, where the programmed and erased states have been measured with a time interval of 10^n s after application of gate bias of −8 and 8 V for 1 s, respectively. The V_{th} values of both programmed and erased states are well maintained for more than 10^5 s. Measurements were carried out to study the V_{th} variation of programmed and erased states under various bending radius of curvatures.[47] Our memory devices exhibited excellent mechanical properties during the bending test. The measurement on V_{th} variation of programmed and erased states *versus* various tensile and compressive bending radii have been included in the Supporting Information (Figure S6). Negligible changes in V_{th} of programmed and erased states were observed for various bending radii even for a radius as small as ∼5 mm. In addition, we recorded V_{th} of programmed and erased states at various bending cycles under a radius of curvature of 10 mm. Both the p-type and n-type flexible flash memory devices based on $AuCl_3$ doped rGO with 25 s duration exhibited almost no degradation of V_{th} even after 500 bending cycles as shown in Figure 4e,f.

CONCLUSION

In summary, we first presented a low voltage flexible flash memory with tunable memory characteristics based on pristine rGO and chemical doped rGO floating gates. Gradient increase in work function of rGO has been achieved *via* direct immersion of rGO monolayer into $AuCl_3$ aqueous solution for various durations. The UPS results show that chemical doping of rGO with $AuCl_3$ causes the Fermi level down-shift up to 0.6 eV which is attributed to the hole doping process from Au NPs. By proper energy band engineering, a huge enhancement in the memory window has been achieved. With the pristine rGO, doped rGO with $AuCl_3$ for 5 and 25 s as floating gates, memory windows of 0.7, 1, and 2.7 V for p-channel flash memories and 0.3, 1.1, and 2.4 V for n-channel flash memories have been obtained, respectively. Meanwhile, various V_{th} can be achieved in both p- and n-type memory devices fabricated on rGO with various doping concentration of $AuCl_3$. The coactivation of enhanced work function of rGO, increased size and density of reduced Au NPs, interfacial dipole formation between Au NPs and rGO film and trapped positive charge carriers assisted p-doping of rGO films are proposed to elucidate the tunable memory characteristics of memory devices based on rGO with chemical doping. We believe that $AuCl_3$ doped rGO based flexible flash memory modules would help to bring future electronics a step closer to controllable device operation modes for practical applications.

METHODS

Materials. The following materials were obtained from Aldrich: auric acid ($HAuCl_4 \cdot 3H_2O$), graphite powder, 3-aminopropytriethoxysilane (APTES), pentacene and $F_{16}CuPc$ (sublimated grade). All chemicals and solvents were used without further purification.

Synthesis and Characterization of rGO Sheets. Graphite oxide was synthesized from graphite by Hummer's method. A total of 12.5 mg as-synthesized graphite oxide was suspended in 25 mL of DI water to create 0.05 wt % brown dispersion. Exfoliation of the graphite oxide to graphene oxide (GO) was achieved by ultrasonication for 1 day. The resulting homogeneous dispersion was mixed with another 25 mL of DI water containing hydrazine (weight ratio of hydrazine to graphene oxide of 7:10) and ammonia. The mixture was refluxed in a water bath around 95 °C for 1 h.

Preparation and Characterization of $AuCl_3$-Doped rGO Double Floating Gate. PET substrate with 30 nm Al_2O_3 was immersed in a solution of APTES (12.5 μL of APTES in 10 mL ethanol) for 45 min at room temperature. Excess, nonreacted APTES molecules were removed by rinsing in ethanol three times and dried under nitrogen gas. The positively charged rGO suspension (0.25 mg mL^{-1}) was first dispensed onto the modified flexible substrates and allowed to self-assemble for 2 min prior to spin-coating at 3000 rpm for 30 s to form rGO monolayer. After rGO monolayer growth, the sample was immersed into $AuCl_3$ aqueous solution with a concentration of 5 mM for various durations. Then the sample was rinsed with DI water and blow-dried with nitrogen gas. The pristine rGO sheets monolayer and doped rGO sheets monolayer were measured using atomic force microscope (AFM, VEECO Multimode V). All photoemission experiments were performed in a VGESCALAB 220i-XL UHV surface analysis system with a base vacuum of 10^{-10} Torr. The samples were prepared onto the heavily doped n-type precleaned silicon substrate outside then transfer into the chamber. For the XPS measurement, a monochromatic Al Kα X-ray source (1486.6 eV) was used to study the energy level changes and possible interfacial chemical reactions across the interface. For UPS measurement, a He discharge lamp (21.2 eV) with an instrumental energy resolution of 90 meV as estimated from the Fermi edge of a cleaned Au was used to measure the work function of the samples. For efficient collection of secondary electrons, samples were negatively biased at −5.0 V with respect to ground.

Device Fabrication. Memory devices were fabricated on 200 μm PET film with 25 nm thermal evaporated Ag as gate electrode. Al_2O_3 layers were deposited using a Savannah 100 ALD system at a substrate temperature of 80 °C. Details of fabricating p-channel and n-channel flexible flash memories are described in Supporting Information. A 40 nm thick pentacene and 30 nm thick $F_{16}CuPc$ were deposited as p-type and n-type semiconductor layer at a rate of 0.1 Å s^{-1} under a base pressure of 2×10^{-6} Torr. Thirty nanometers thick gold electrodes were thermally evaporated through a shadow mask with a channel length (L) of 50 μm and width (W) of 1000 μm. The electrical characteristics of all the devices were measured using a Keithley 2612 source meter at room temperature in ambient conditions.

Conflict of Interest: The authors declare no competing financial interest.

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Supporting Information Available: The AFM image for rGO sheet, Raman spectra of rGO and GO, AFM image of rGO doped with $AuCl_3$ for 45 s, XPS data (metal peak) of pristine rGO film, the memory characteristics of high voltage device, program/erase speed of flash memories and threshold voltages with respect to the various bending radius. This material is available free of charge *via* the Internet at http://pubs.acs.org.

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